REMARKS

The present application was filed on April 6, 2007 with claims 1-31. Claims 1-31 remain pending.

In the present Office Action, the Examiner has rejected claims 1-5, 7-15 and 17-31 under 35 U.S.C. §103(a) as being unpatentable over Reiner (WO 2004/053889) in view of Lee (United States Patent No. 5,257,225) and Doyle et al. (U.S. Publication: "Characterization of Oxide Trap and Interface Trap Creation During Hot-Carrier Stressing of n-MOS Transistors Using the Floating-Gate Technique"; hereinafter Doyle).

The Examiner has indicated that claims 6 and 16 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

In this response, Applicants respectfully traverses the rejections. Applicants respectfully request reconsideration of the present application in view of the remarks to follow.

Independent Claims 1, 11, 21, 24 and 27

Independent Claims 1, 11, 21, 24 and 27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Reiner in view of Lee and Doyle et al.

Reiner with respect to Claims 1 and 2

Applicants respectfully traverse the §103(a) rejection of claims 1 and 2 on the ground that there is insufficient objective evidence of motivation to combine Reiner and Lee or Reiner and Doyle in a manner that meets the limitations of the claims at issue, as discussed further below.

Regarding claims 1 and 2, the Examiner states that Reiner teaches programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistors, wherein the hot carrier aging technique comprises injection of carriers into a gate oxide. The Examiner further states that Reiner (page 5, line 19 to page 6, line 19) discloses thermally damaging the drain junction of T2 by inducing hot carriers at the drain/oxide/gate junction. The Examiner further states that Reiner (page 7, lines 7 to 11) discloses gate oxide breakdown as induced by hot carriers or hot carriers thermally damaging a drain junction.

Applicants disagree with these statements. Reiner does not disclose *programming* using *hot carriers*, but, rather, discloses *thermally damaging the drain junction*. Reiner states that "a MOS transistor is employed as memory; this memory transistor can be *programmed* by being

brought itself into a snap-back mode, in which a drain junction of the transistor is thermally damaged." (Reiner: page 2, lines 13-16). Reiner further states that "The device further comprises programming means for applying predetermined voltages …, which applied voltages force the memory transistor into a snap-back mode resulting in a current thermally damaging the drain junction of the memory transistor." (Reiner: page 2, lines 4-8), "The programming of the memory transistor results in a leakage in the transistor, which can be detected in the form of a leakage current in a subsequent readout. It should be ensured in the readout that a detected leakage is indeed caused by a hard drain fusing which results in a damaged connecting the drain with the source diffusion" (Reiner: page 4, lines 14-18), and "Hot carrier conditions resulting in a degradation, however, are avoided effectively with the proposed programming cycle comprising a ramping down of the voltage applied to the gate of the memory transistor." (Reiner: page 4, lines 7-9). *Therefore, Reiner does not teach hot carrier aging techniques for programming a memory cell.*

Furthermore, Reiner makes clear that the gate oxide breakdown referred to (page 7, lines 7 to 11) does not program a memory cell. Reiner states "Therefore, the proposed memory is insensitive to gate oxide breakdown" (Reiner: page 7, lines 10 and 11). Reiner is clear that drain damage, not gate oxide breakdown, is the programming mechanism for the memory cell. Reiner never mentions hot carrier programming or the injection of any carriers into a gate oxide. Therefore, Reiner does not disclose or suggest that a hot carrier aging technique comprises injection of carriers into a gate oxide to program a memory cell.

The Examiner states that Reiner teaches at page 7, lines 7-11 oxide breakdown as obviously induced by degradation by hot carrier mechanism: trapping electrons. Applicants disagree. Reiner never mentions or teaches oxide breakdown related to hot carriers, hot carrier mechanisms, degradation by hot carrier mechanisms, trapping electrons or traps.

Applicants again note that Reiner teaches:

> In an equally preferred embodiment of the invention, a programming voltage level above the normal operation voltage level is used, in order to keep the cell size reasonably small. *High voltage levels may result in a degradation of the memory device due to an increased heating of the carrier. Hot carrier effects occur e. g. in strong pinch-off conditions in a transistor, which in turn occur with a high drain voltage and a moderate to low gate voltage at the transistor. It has thus to be ensured that no intolerable degradation of the memory circuitry occurs*

due to the proposed high programming voltage. Hot carrier conditions resulting in a degradation, however, are ***avoided effectively*** *with the proposed programming cycle comprising a ramping down of the voltage applied to the gate of the memory transistor.*
(Page 3, line 31, to page 4, line 9; emphasis added.)

Thus, contrary to the Examiner's assertion, Reiner does *not* disclose or suggest *programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor.* In fact, Reiner actually **teaches away** from the present invention by teaching to *avoid hot carrier conditions.*

Lee and Doyle

Furthermore, in the text cited by the Examiner, Lee teaches that "the fact that wordline pulse 65 ramps up is significant is that the small Fowler-Nerdheim current at the beginning which fills up the traps in the thin dielectric region before the higher Fowler-Nerdheim current will reduce the stress on the tunneling window dielectric and improve the dielectric lifetime." (Col. 4, line 67, to col. 5, line 4.) Lee, however, does not disclose or suggest *programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor.*

Finally, Doyle does not disclose or suggest *programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor.*

Thus, even as combined in the manner suggested by the Examiner, Reiner, Lee and Doyle, alone or in combination, *do not teach every element of the independent claims.* Furthermore, based on the KSR considerations discussed hereinafter, the combination/modification suggested by the Examiner is not appropriate.

KSR Considerations

An Examiner must establish "an apparent reason to combine … known elements." *KSR International Co. v. Teleflex Inc. (KSR)*, 550 U.S. ___, 82 USPQ2d 1385 (2007). Here, the Examiner merely states that it would have been obvious to incorporate the teachings (that the injection of carriers causes at least one of, the creation of traps, and the filling of traps) by Lee and Doyle in the cited claim limitation rejection. The Examiner asserts that the suggestion/motivation would have been obvious to one of ordinary skill in the art to conclude

that (the) injection of carriers, as induced by voltage/current biasing of a transistor device, can cause oxide degradation resulting in charge trapping.

Applicants, however, are claiming a new technique for programming a one time programmable memory. There is no suggestion in Reiner, Lee and Doyle, alone or in combination, to *program a transistor using a hot carrier transistor aging technique to alter a characteristic of the transistor.*

Furthermore, Reiner's teaching to *avoid hot carrier conditions* ***teaches away*** from the present invention. The *KSR* Court discussed in some detail United States v. Adams, 383 U.S. 39 (1966), stating in part that in that case, "[t]he Court relied upon the corollary principle that when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be nonobvious." (KSR Opinion at p. 12). Thus, there is no reason to make the asserted combination/modification.

Additional Claims

Applicants respectfully disagree with Examiner's rejections of independent claims 11, 21 and 27, and dependent claim 25 at least for the same reasons as Applicants present for claims 1 and 2.

In rejecting independent claim 24, the Examiner recites that Reiner teaches a memory cell comprising only one transistor. Claim 24 recites a "memory cell, *comprising only one transistor*." The Examiner cites page 5, line 9 and T2 of FIG. 1. Applicants disagree and note that Reiner states "The memory cell comprises a selection transistor T1 and a memory transistor T2." (Reiner: page 5, lines 8 and 9). Furthermore, Reiner states "FIG. 1 schematically illustrates a memory cell of a memory device according to the invention" (Reiner: page 5, lines 3 and 4). FIG. 1 clearly shows two transistors, T1 and T2, within the illustrated memory cell. Thus, the memory cell of Reiner does not comprise only one transistor, but comprises two transistors.

Independent claim 27 claims an integrated circuit. The Examiner in rejecting claim 27 does not present any teachings or disclosure of an integrated circuit. At least because the Examiner does not present a teaching or disclosure of an integrated circuit, the Applicants believe that claim 27 is in condition for allowance.

In rejecting claims 3, 13, 23 and 29, the Examiner recites that "Reiner teaches said altered characteristics is a change in a threshold voltage of said at least one of said transistors (page 6,

lines 27-31 teach that T2 of FIG. 1, when not programmed in a reading operation, will not conduct current; yet when T2 is programmed, in contrast, it will conduct current, obviously changing the threshold voltage of the memory T2)." Applicants disagree and note that Reiner states "a current should flow through the cell even though the memory transistor T2 is turned off, since the fused drain junction of the memory transistor T2 allows a leakage current to pass" (Reiner: page 6, lines 29-31). Applicants further note that Reiner states "while in a programmed state of the memory cell, the drain junction of the memory transistor T2 is thermally damaged." (Reiner: page 5, lines 17-18). Therefore, the current conducted is not due to a change in threshold voltage, but to drain leakage current caused by the fused drain. As is known in the art, threshold voltage is the gate voltage at which channel conduction occurs between the source and drain of the transistor. Threshold voltage is not a voltage at which drain leakage occurs. Therefore Reiner does not teach said altered characteristic is a change in a threshold voltage.

In rejecting claims 4 and 14, the Examiner recites that Reiner teaches said programming step further comprising the step of applying a stressful voltage to a drain and a gate of said at least one of said transistors to cause said change in said threshold voltage of said of said at least one of said transistors (page 5, line 7 to page 7 line 6). Applicants disagree and note that the only stressful voltage applied is to a drain, not a gate. Reiner states "The programming voltage Vprog is set to a level exceeding the allowed maximum operating voltage" (Reiner: page 5, lines 24-25). FIG. 1 of Reiner shows Vprog applied to the drain of T1. Reiner further states "For programming a memory cell, the voltages Vsel and Vctrl applied to the gate of the selection transistor T1 and to the gate of the memory transistor T2, respectively, are set by programming means (not shown) to a voltage level predetermined for programming." (Reiner: page 5, lines 19-22). Applicants note that Reiner does not mention a stressful voltage applied to a gate. Furthermore, as noted with respect to claim 3, Reiner does not teach a change in threshold voltage. Thus, Reiner does not teach programming comprising applying a stressful voltage to a drain and a gate of a transistor to cause a change in threshold voltage of the transistors.

In rejecting claims 5, 15 and 30, the Examiner recites that Reiner teaches the step of detecting said programmed at least one of said transistor by sensing said change in said threshold voltage of said at least one of said transistors (page 6, line 27 to page 7 , line 6). Per Applicants argument set forth regarding claims 3 and 4 above, Reiner does not teach a change in threshold

voltage. Furthermore, Reiner does not teach a detection of a change in threshold voltage. On page 6, line 27 to line 31, Reiner teaches the change in current is due to leakage of the fused drain junction of T2, not a change in threshold. Reiner states "since the fused drain junction of the memory transistor T2 allows a leakage current to pass. The amount of current flow is detected" (Reiner: page 6, lines 30 to page 7, line 1). Thus, Reiner does not teach detecting said programmed at least one of said transistors by sensing said change in said threshold voltage of said at least one of said transistors.

In rejecting claims 7, 17 and 31, the Examiner recites that Reiner teaches that said altered characteristic is a change in a saturation current of said at least one of said transistors (page 6, lines 26 to page 7, line 6). Reiner does not mention or teach saturation current. Reiner teaches the altered characteristic is a change in drain leakage current. Reiner states "a current should flow through the cell even though the memory transistor T2 is turned off, since the fused drain junction of the memory transistor T2 allows a leakage current to pass" (Reiner: page 6, lines 29-31). Applicants further not that Reiner states "while in a programmed state of the memory cell, the drain junction of the memory transistor T2 is thermally damaged." (Reiner: page 5, lines 17-18). Thus Reiner does not teach said altered characteristic is a change in a saturation current of said at least one of said transistors.

In rejecting claims 8 and 18, the Examiner recites that Reiner teaches said programming step further comprising the step of applying a stressful voltage to a source and a gate of said at least one of said transistor to cause said change in said saturation current of said of said at least one of said transistors (page 5-6). Applicants disagree and note that the only stressful voltage applied is to a drain, not a gate. Reiner states "The programming voltage Vprog is set to a level exceeding the allowed maximum operating voltage" (Reiner: page 5, lines 24-25). FIG. 1 shows Vprog applied to the drain of T1. Reiner further states "For programming a memory cell, the voltages Vsel and Vctrl applied to the gate of the selection transistor T1 and to the gate of the memory transistor T2, respectively, are set by programming means (not shown) to a voltage level predetermined for programming." (Reiner: page 5, lines 19-22). Applicants note that Reiner does not mention a stressful voltage applied to a gate. Furthermore, as noted with respect to claim 7, Reiner does not teach a change in saturation current. Thus, Reiner does not teach said programming step further comprising the step of applying a stressful voltage to a source and a

gate of said at least one of said transistors to cause said change in said saturation current of said of said at least one of said transistors.

In rejecting claims 9 and 19, the Examiner recites that Reiner teaches the step of detecting said programmed at least one of said transistors by sensing said change in said saturation current of said at least one of said transistors (page 6-7). Per Applicants argument set forth regarding claims 7 and 8 above, Reiner does not teach a change in saturation current. Furthermore, Reiner does not teach a detection of a change in saturation current. In page 6, line 27 to line 31, Reiner teaches the change in current is due to leakage of the fused drain junction of T2, not a change in saturation current. Reiner states "since the fused drain junction of the memory transistor T2 allows a leakage current to pass. The amount of current flow is detected" (Reiner: page 6, lines 30 to page 7, line 1). Thus, Reiner does not teach detecting said programmed at least one of said transistors by sensing said change in said saturation current of said at least one of said transistors.

In rejecting claims 10 and 20, the Examiner recites that Reiner teaches said detecting step further comprises the steps of raising the gate terminal of each transistor in a selected row to a positive potential and evaluating a rate of voltage decay if at least one column in said array of transistors (page 6, lines 22-23). Reiner does not teach or mention rows or raising the gate terminal of each transistor in a selected row. Thus, Reiner does not teach raising a gate terminal of each transistor in a selected row to a positive potential.

Applicants disagrees with the rejection of claims 12 and 28 by the Examiner, for at least the reason that, as discussed above with respect to claims 1 and 2, Reiner does not teach or disclose programming by applying a stressful voltage to cause hot carrier transistor aging.

Furthermore, dependent claims 2-10, 12-20, 22-23, 25-26 and 28-31 are patentable at least by virtue of their dependency upon independent claims 1, 11, 21, 24 and 27 as well as for reasons presented above.

In light of the above remarks and amendments, Applicants respectfully submit that claims 1-31 are in condition for allowance and request the withdrawal of the §103(a) rejections.

Respectfully submitted,

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